## **CLAIMS**

## WHAT IS CLAIMED IS:

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1. A method of manufacturing an integrated circuit, comprising:
providing an amorphous semiconductor material including
germanium above a bulk substrate of semiconductor material;

annealing the amorphous semiconductor material to form a single crystalline semiconductor layer containing germanium; and

doping the single crystalline semiconductor layer and the substrate at a source location and a drain location to form a source region and a drain region, whereby a channel region between the source region and the drain region includes a thin semiconductor germanium region.

- 2. The method of claim 1 further comprising:
  before the doping step, providing a cap layer above the amorphous semiconductor layer.
- 3. The method of claim 2 further comprising:
  after the providing a cap layer step, providing a gate structure
  between the source location and the drain location.
- 4. The method of claim 3, wherein the cap layer is an amorphous semiconductor layer.
  - 5. The method of claim 4, further comprising: before the doping step, annealing the cap layer.
- 6. The method of claim 4, wherein the amorphous semiconductor layer includes silicon.
- 7. The method of claim 1, wherein the bulk substrate includes single crystalline silicon.



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8. The method of claim 1, wherein the amorphous semiconductor layer observation includes silicon germanium.

- 9. The method of claim 7, wherein the amorphous semiconductor layer includes silicon germanium
- 10. The method of claim 9, wherein the annealing step takes place at a temperature sufficient to melt the amorphous semiconductor layer and is below the melting temperature of the substrate.
- 11. The method of claim 10, wherein the annealing step is performed by an excimer laser.

12. A method of manufacturing an ultra-large scale integrated circuit including a transistor, the method comprising steps of:

depositing an amorphous silicon germanium material above a top surface of a semiconductor substrate;

annealing the amorphous silicon germanium material;
depositing an amorphous silicon material above the silicon germanium material;

annealing the amorphous silicon material; and providing a source region and a drain region for the transistor, the source region and the drain region being deeper than a combined thickness of the silicon germanium material and the silicon material.

- 13. The method of claim 12, further comprising:

  providing a gate structure before providing a source region and a drain region step.
- 14. The method of claim 12, further comprising:

  providing an oxide layer over the silicon material after the second annealing step.

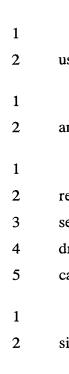


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1	15. The method of claim 12, wherein the silicon germanium material is a		
2	single crystalline layer after the first annealing step.		
1	16. The method of claim 12, wherein the silicon material is a single		
1			
2	crystalline layer after the second annealing step.		
1	17. The method of claim 12, wherein the silicon material is 100-150Å		
2	thick.		
1	18. The method of claim 12, wherein the annealing temperature for the		
2	first and second annealing steps is at or above 1100°C and below 1400°C.		
1	A process of forming a transistor with a silicon germanium channel		
2	region, the process comprising:		
3	depositing a thin amorphous silicon germanium material above a top		
4	surface of a semiconductor substrate;		
5	annealing the silicon germanium material to form single crystalline		
6	silicon germanium material;		
7	depositing a thin amorphous silicon material above the single		
8	crystalline silicon germanium material;		
9	annealing the silicon material to form single crystalline silicon		
10	material; and		
11	providing a source region and a drain region for the transistor, the		
12	source region and the drain region extending into the substrate.		
1	20. The process of claim 19, wherein the silicon germanium material is		
2	200-500Å thick.		
1	21. The process of claim 20, wherein the silicon material is 100-150Å		
2	thick.		
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1	22. The process of claim 19, wherein the annealing steps are excimer		

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laser annealing steps.



23.	The process of claim 22, wherein the excimer laser annealing steps
use a wavelen	igth of 308 nanometers.

- 24. The process of claim 23, the source and drain regions each including an extension.
- A transistor comprising a source and drain region and a channel region, the source and drain regions being at least partially disposed in a bulk semiconductor substrate, the channel region being disposed between the source and drain regions, the channel region including a silicon germanium layer and a silicon cap layer.
- 26. The transistor of claim 21, wherein the source and drain regions are silicided to eliminate any effect of germanium in the source and drain regions.

